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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,119	07/03/2003	Dean Nobunaga	400.239US01	7175

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EXAMINER	
ELAMIN, ABDELMONIEM I	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,119	NOBUNAGA, DEAN	
	Examiner	Art Unit	
	A Elamin	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin, US. Pat. No. 6,839,860.

3. Claims 1, Lin teaches a fast data access circuit [*the circuit of Fig. 2*], having a standard clock input signal [*CLKIN of Fig. 2*], comprising:

a clock delay circuit that provides a selectable time delay to the standard clock input signal to produce a delayed clock signal [*slave DLL 114 of Fig. 2*];

a control circuit that generates a mode control signal [*SEL 156 of Fig. 2*];

a multiplexing circuit having a first input coupled to the standard clock input signal and a second input coupled to the delayed clock signal [*MUX 116 of Fig. 2*], the multiplexing circuit outputting a selected clock in response to the mode control signal [*see Fig. 2*]; and

a data output register, coupled to the multiplexing circuit and an input data bit, for outputting the input data bit in response to the selected clock [*130 of Fig. 2*].

4. Claim 2, Lin teaches the data output register is a data first-in-first-out (FIFO) register [*inherently, a FIFO is used to buffer output data*].

5. Claim 3, Lin teaches a data FIFO register control logic, coupled between the multiplexing circuit and the data FIFO register, for generating FIFO control signals in response to the selected clock [*clock tree circuit 170 of Fig. 2, col. 4, lines 21-32*].

6. Claims 4, Lin teaches the control circuit comprises a mode/configuration register that generates the mode control signal in response to a loaded configuration word [*generating shifting signals to controller 146 of Fig. 5 to adjust the amount of delay applied to the CLCIN, see Fig. 5, col.6, lines 32-37*].

7. Claims 5, 6, 8-11, 12, 14, 18-19 and 20-22, Lin teaches the loaded configuration word is in response to a frequency of the standard clock input signal [*the configuration word is produced by signal detector in response to the frequency of CLKIN, see Fig. 5, col.6, lines 32-37*];

wherein the selectable time delay is selected in response to the loaded configuration word [*col.6, lines 32-37*].

8. Claims 7, Lin teaches the input data bit is part of a data stream from a memory array [*see data 124 of Fig. 2and related disclosure*].

9. Claims 13, Lin teach each of the plurality of delay circuits comprises a plurality of inverter gates [*see Fig. 5*].

10. Claims 15, Lin teaches a burst counter for generating a plurality of sequential addresses, within a predetermined address range, to the array of memory cells such that a plurality of data is accessed within the predetermined address range [*Figs. 7 and 8, col. 7, lines 30-45, 60 thru col. 8, line 6*].

11. Claims 16, Lin teaches data output register control logic that generates a plurality of data output register control signals from the selected clock signal [*clock tree circuit 170 of Fig. 2, col. 4, lines 21-32*].

12. Claims 17, Lin teaches the data rate is determined by the data output register control signals [*col. 4, lines 21-32*].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A Elamin whose telephone number is (571) 272-3674. The examiner can normally be reached on MON-FRI 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A Elamin
Primary Examiner
Art Unit 2116

February 16, 2006